

**Presenter: Stephen Mancini, SUNY Poly PhD Candidate**

**Title:** Integration of Room Temperature Implantation for 4H-SiC Based Power Devices Through Process Optimization and Device Design

**Abstract:** Although 4H-SiC is a preferred material for high voltage devices due to its wide bandgap, the material itself provides unique challenges in processing techniques that are not seen in traditional Silicon devices. Ion implantation of Aluminum (Al) in conventional 4H-SiC technology is performed at elevated temperatures to mitigate lattice damage such as the formation of Basal Plane Dislocations (BPDs) that can lead to device degradation under high bipolar current stress. Due to the many processing benefits, there has been a push to implement room temperature ion implantation without generating severe BPDs generation, and while a critical dose has previously been reported, a detailed study of the impact of implantation energy and dose altogether, i.e., the profile, was not studied in greater detail. By optimizing the overall dopant profile, potential BPD generation from RT implantation can be mitigated and thus device reliability and lifetime would improve. Longevity of devices can be improved even when BPDs are located within a device by suppressing BPD expansion and subsequent degradation. By utilizing unipolar devices such as JBS diode integrated MOSFETs (JBSFETs) bipolar recombination can be eliminated increasing overall reliability, however optimization of these devices are needed to compete with traditional co-packaged MOSFETs.