“Leveraging Memristors in Spiky Neuromorphic Computing Systems”

Garrett S. Rose, Ph.D.
University of Tennessee, Knoxville

Abstract:
Although CMOS technology scaling does continue to march forward, it is also true that a significant slow-down in such scaling has occurred in recent years. This slower pace of technology advancement also means that modern computer systems can no longer rely exclusively on scaling for performance enhancements. Now is the time for circuit and system designers to consider alternative approaches to computer system architectures. One such approach is neuromorphic computing which uses models for biological neural systems to construct brain-inspired computer systems. Two basic components are required for a typical neuromorphic system: neurons that fire based on spike patterns received and synapses that provide weighted connections between neurons. Here we consider spiky neuromorphic systems where neurons are implemented using analog/mixed-signal CMOS and synapses are built from memristors (e.g. ReRAM). The specific neuromorphic framework presented also allows for recurrent pathways in the networks constructed, a feature that is particularly useful for stateful neuromorphic processing. One such spiky recurrent neuromorphic system is mrDANNA (Memristive Dynamic Adaptive Neural Network Array), a hybrid CMOS/memristor implementation resulting from collaborations between the University of Tennessee and SUNY Polytechnic Institute. A full mrDANNA system offers the potential to construct small neural network applications operating on a fraction of the power consumed by analogous deep learning systems.

Bio:
Garrett S. Rose has been an Associate Professor in the Department of Electrical Engineering and Computer Science at the University of Tennessee since 2014. He received the B.S. in Computer Engineering from Virginia Tech in 2001. He recceived the M.S. and Ph.D. degrees in Electrical Engineering from the University of Virginia in 2003 and 2006, respectively. From 2006 through 2011 he was an Assistant Professor with the Electrical and Computer Engineering Department at Polytechnic University (now NYU Polytechnic School of Engineering) in Brooklyn, NY. From 2011 through July 2014 he was a Senior Electronics Engineer with the Air Force Research Laboratory, Information Directorate in Rome, NY. Through his career, his research interests have been focused in the area of nanoelectronic circuit design as applied to a range of applications, including reconfigurable computing, neuromorphic computing and hardware security.