

Nanosheets

Nicolas Loubet, Ph.D.

IBM

Abstract:

Horizontally stacked GAA Nanosheet structures can answer logic device needs at 5nm technology nodes and beyond. They offer excellent electrostatics and short channel control, can be fabricated with minimal deviation from FinFET, and circumvent some of the patterning challenges associated with scaled technologies. Additionally, Nanosheet device architecture enable the best CMOS logic power and performance trade-off and provide additional area and gate length (L_g) scaling benefits at the 5nm node and beyond. The improved electrostatics of GAA devices and additional design flexibilities, which allow a continuous range of active widths (W_{eff}) in NS devices, open new opportunities in term of power/performance optimization with co-integration of logic and SRAM. Stacked Nanosheets are fabricated with minimal deviation compared to the industry standard FinFET device integration, with a significant reuse of legacy integration and manufacturing knowledge. We will review the benefits of using this technology for mobile and High Performance computing and discuss the fabrication challenges associated with the Nanosheet specific modules.

Bio:

Nicolas Loubet received the B.S. and M.S degrees in physics from Paul Sabatier University, Toulouse (Fr.), in 2000 and 2001. In 2003, he received a high-level Engineering degree in the field of Physics and Microelectronics from the National Institute of Applied Sciences (INSA) in Toulouse, and the PhD degree in the domain of Materials, Technology and Electronic Devices in 2006.

From 2003 to 2008, he joined STMicroelectronics Research and Development group in front-end materials and epitaxy where he was engaged in the development of Advanced Epitaxy of Si and SiGe materials, and developed the HCl vapor-phase etching of SiGe for the fabrication of silicon-on-nothing (SON) and dielectric isolation transistors. In 2008, he joined the Silicon Technology Research Alliance at IBM Research in Albany, NY and the following years, his research focused on Junction and Strain module engineering for the 20nm, 14nm, 10nm, and 7nm CMOS device nodes using strained SOI and SGOI, SiGe relaxed buffer and ultra-low resistivity SiGe:B and SiC:P for FDSOI and FinFET devices on Bulk and SOI substrates.

In 2015, he became a Senior Engineer and Technical Leader at IBM Research where his research focused on material, process, and device integration of Gate-All-Around devices for 5nm CMOS technology and beyond. In 2017, he was first author of IBM 5nm Technology paper and Press Release "Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET".

Since 2018, he is manager of the Front-End Of Line (FEOL) Process Development team at IBM Research with a focus on materials research and process development for leading edge CMOS logic devices. He has published more than 100 papers in journals and conference proceedings, and the holder of more than 250 patents in the domain of epitaxy, device and process integration.